English Translation
of
DE 37 44 128

(19) **FEDERAL REPUBLIC OF GERMANY**

[Seal]

GERMAN PATENT OFFICE

(12) **Offenlegungsschrift [Unexamined]**

(10) **DE 3,744,128 A 1**

(21) File number: P 37 44 128.0
(22) Filing date: December 24, 1987
(43) Publication date: July 13, 1989

(51) Int. Cl. [4]:
G 06 F 13/28
G 11 C 13/08
// G01J 3/06

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Examination request pursuant to § 44 PatG [Patent Code] has been filed.

(54) Method and Circuit Arrangement for the Programmed Actuation of CCD and Photodiode Matrix Arrays

(57) With the method and the circuit arrangement, semiconductor image sensors will be rapidly actuated by means of a program in order to thus record only the parts of interest of an image. The method does not require the very large memory unit of memory-programmed controls and allows a substantially greater speed of control word generation than do pure processor-managed controls.

With the new method and the associated circuit arrangement, sequences of digital control words are generated rapidly in that a DMA controller loads independently one command block after the other into its register and, after each self-programming, sends out a control word to the image sensor as often as determined by the part of the program loaded at that moment.

Programmed actuation of semiconductor image sensors.

Description

Method and arrangement for the fast memory-programmed digital control of CCD and photodiode matrix arrays.

The invention concerns a method and a circuit arrangement for the fast programmed generation of digital control words and actuation of CCD and photodiode matrix arrays (semiconductor image sensors / semiconductor cameras).

There exist various possibilities for generating these digital control signals. The first possibility is the construction of control circuits, which, by means of inquiry of the state of the target system – for example, an image sensor – generate control signals that are rigidly linked to this state. A second possibility is memory-programmable control. In it, each individual control word of the control sequence is stored in a memory unit. The target system is actuated in such a way that a DMA controller or address counter addresses the memory unit and the control words are thereby applied via the data bus to the target system. In a third method, the control word sequence is programmed in the form of algorithms on a processor and is output directly by it.

The drawbacks of control circuits are their high cost in terms of hardware and their very low flexibility. Memory-programmable controls necessitate a very large memory unit. In addition, externally triggered control program jumps cannot be executed without a time delay. The drawback of a pure processor control is the relatively low speed with which the control words are generated. One possibility of compensating for this is offered by parallel processor structures, which, once again, are very costly.

The invention is based on the object of actuating a semiconductor matrix array in such a way that selected columns and/or rows of an image can be acquired in a targeted manner. Thus, the video signals of all image points will not be output by the semiconductor camera and subsequently the desired information extracted from the total image, but, instead, only preselected image regions are acquired with the sensor. This is helpful, for example, in spectroscopy using semiconductor image sensors, when only certain spectral regions are to be recorded in a very short time. The advantages of a pure memory-programmable control will be combined with the advantages of a processor-managed control without having to put up with the disadvantages of the two methods.

The object is solved in accordance with the invention in such a way that digital control signals are program-generated for the semiconductor image sensor in that one or more DMA controllers that has/have a register structure according to **Fig.** 2 is/are programmed in such a way that a data transfer corresponding to **Fig.** 3 is possible.

Fig. 1 shows the bus structure of the arrangement. A CPU (**1**) programs the main register (**10**) of the DMA controller (**2**) via the bus interfaces (**5**) / (**6**) and the system bus (**8**) and loads channel programs (**12**), consisting of a series of channel blocks (**13**), into the memory unit (**3**). Subsequently, the DMAC independently transfers the first command block – CCB 1 (**13**) – from the memory unit (**3**) into its channel register (**11**). **Fig.** 3 shows the principle of data transfer between memory unit (**3**), DMAC (**2**), and image sensor (**4**). One of the channel registers (**14**) contains the camera control word (**15**); another register determines the number *n* of times the control word is transferred repeatedly. For adjustment of the control signals (**15**) to the respective timing requirements of the semiconductor array (**4**) used, a suitable control circuit (**16**) has to be connected upstream to the array.

The control word transfer is started by an external synchronization signal. When the internal counter of the DMAC has reached the programmed number of transfers, the next command block is loaded from the memory unit into the channel register (**11**) – CCB 2 to CCB *N* (**13**). During this phase, the sensor (**4**) persists in the state that was set by the last control word (**15**). Through the chain of command blocks, it is possible to prepare complex operating programs (**12**) with jumps and loops.

The synchronization between DMAC and sensor is accomplished by use of the DMA transfer signal (**17**) as a sensor clock.

Fig. 4 shows, on the example of the image sensor MC 9256 of the Reticon company, the timing diagram of the input and output signals when image sensor lines that are not to be read are specifically skipped. The master clock (MCLK) is the DMA transfer signal (**17**), by means of which the DMAC and camera are synchronized with each other. It is inactive when command blocks are transferred (CBTR phase). LTRD (line transfer and row clock disconnect), RCLK (row clock), and LT (line transfer) are control bits of the control word (**15**). If LTRD is active (= 1), then the control signals MCLK, RCLK, and LT act directly on the sensor (mode IV). RCLK actuates the internal

shift register and selects out a specific sensor line. The lines that have been skipped are not read out in this case. When the camera line (line N + M) to be acquired is addressed, activation occurs with a new control word *LT*. In this way, a complete line is transferred into a readout register. Subsequently, with the MCLK, the video signals of the lines are read out in series.

The method and the circuit arrangement form a digital control that, in connection with semiconductor image sensors, is superior to controls according to other methods. With it, complex and long control word sequences can be generated. For this, substantially less memory capacity is required than for memory-programmable controls. The speed of the generation of control signals, however, is comparable here to their higher output speed. The control can also be simply programmed by an external computer and triggered at specific times through events from the outside. The arrangement of the invention can be realized at a relatively low technical cost.

Patent Claims

1. A method and arrangement for the programmed actuation of CCD and photodiode matrix arrays, hereby **characterized** in that one or more DMA controllers generate sequences of digital control words.
2. The method and arrangement according to claims 1, further characterized in that the individual DMA controller outputs the content of one or more internal registers, these register contents being the control words to be generated.
3. The method and arrangement according to claims 1 and 2, further characterized in that a register content can be output several times in succession, it being possible to program the number of output operations.
4. The method and arrangement according to claims 1 to 3, further characterized in that, during the output of the control word, the DMA controller or controllers generates or generate a control signal that is synchronous to this output.

5. The method and arrangement according to claims 1 to 4, further characterized in that the control words are edited by a logic connected downstream to the DMA controller and are linked to the synchronization signal.

6. The method and arrangement according to claims 1 to 3, further characterized in that the DMA controller is connected with one or more memory units and independently loads its register contents from these memory units.

7. The method and arrangement according to claims 1 to 6, further characterized in that interfaces exist between DMA controller, memory unit, semiconductor array, and external computer, which make possible a selective blocking and relay of signals in various operational phases.

8. The method and arrangement according to claims 1 to 7, further characterized in that the memory unit and the DMA controller are programmed by an external computer.

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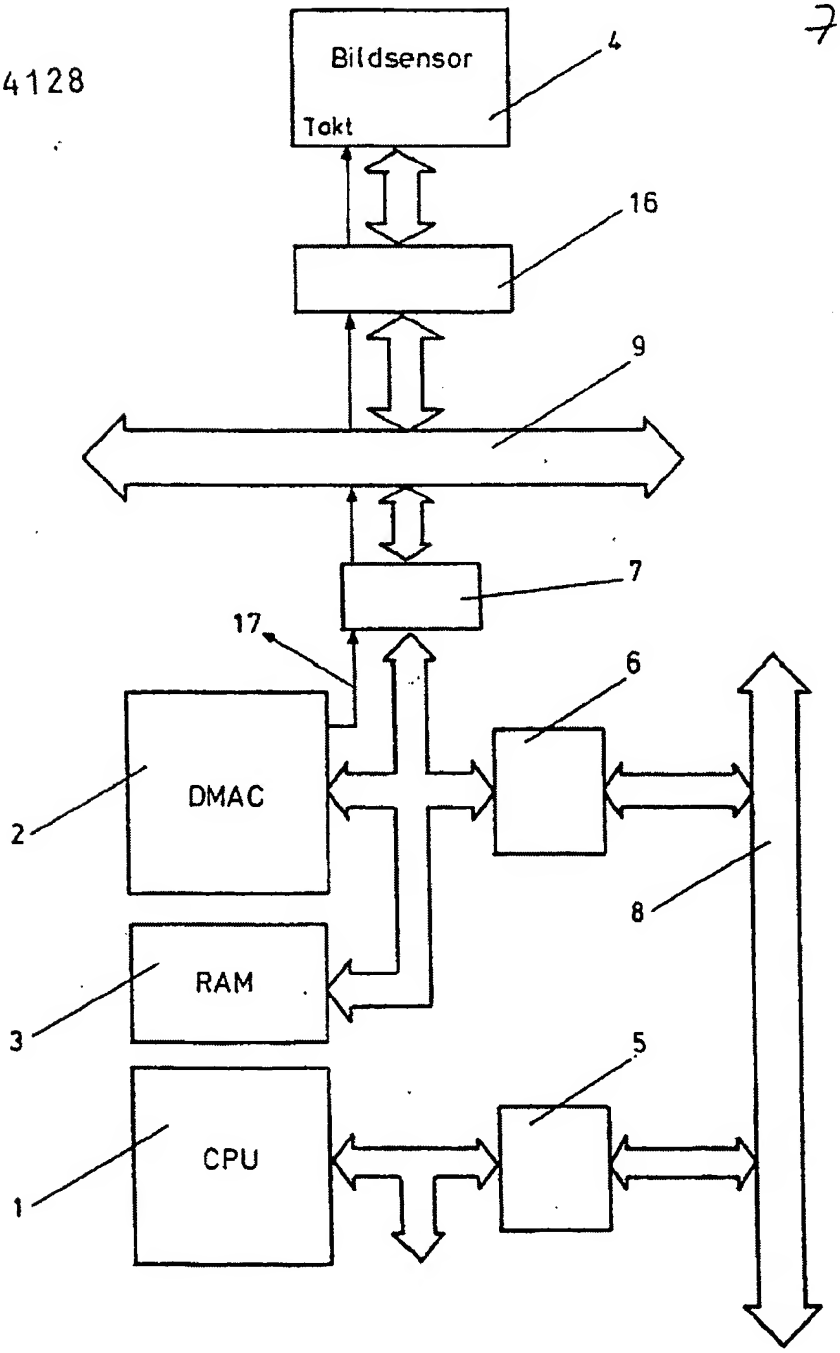


Fig. 1

Bildsensor	=	image sensor
Takt	=	clock

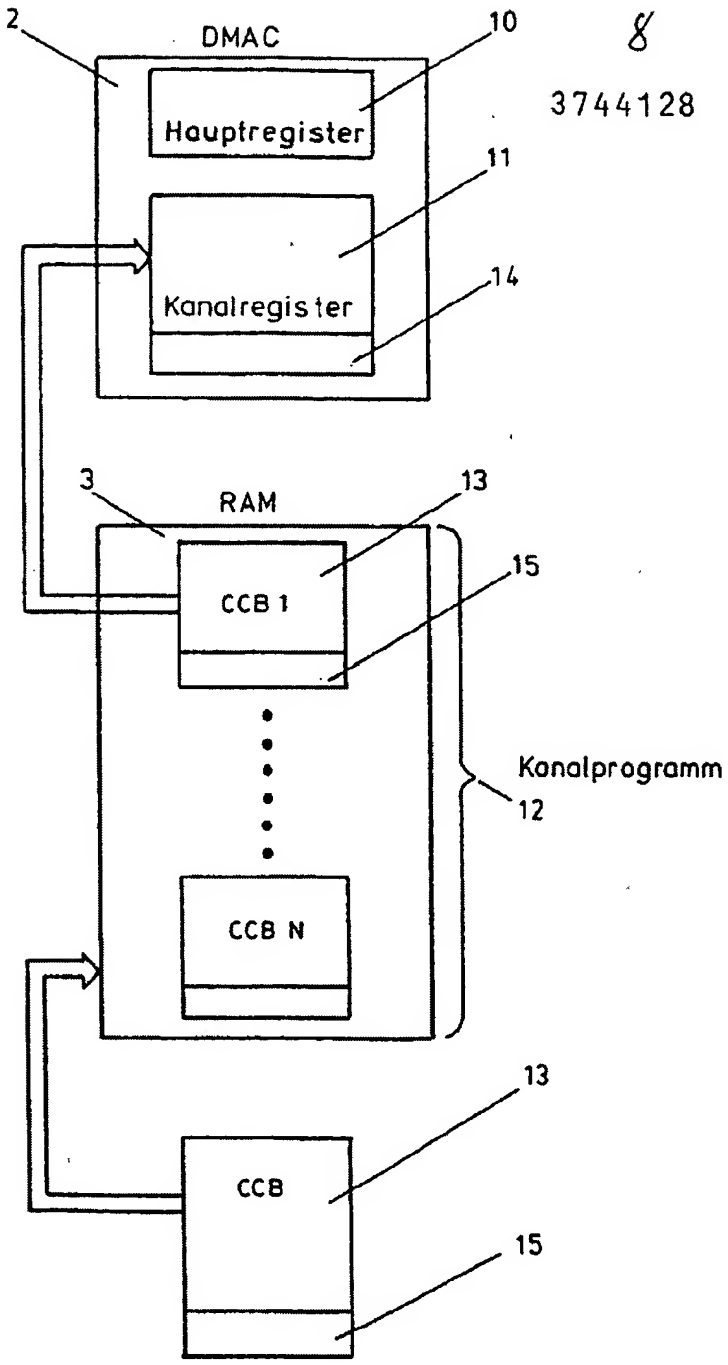


Fig. 2

Hauptregister	=	main register
Kanalregister	=	channel register
Kanalprogramm	=	channel program

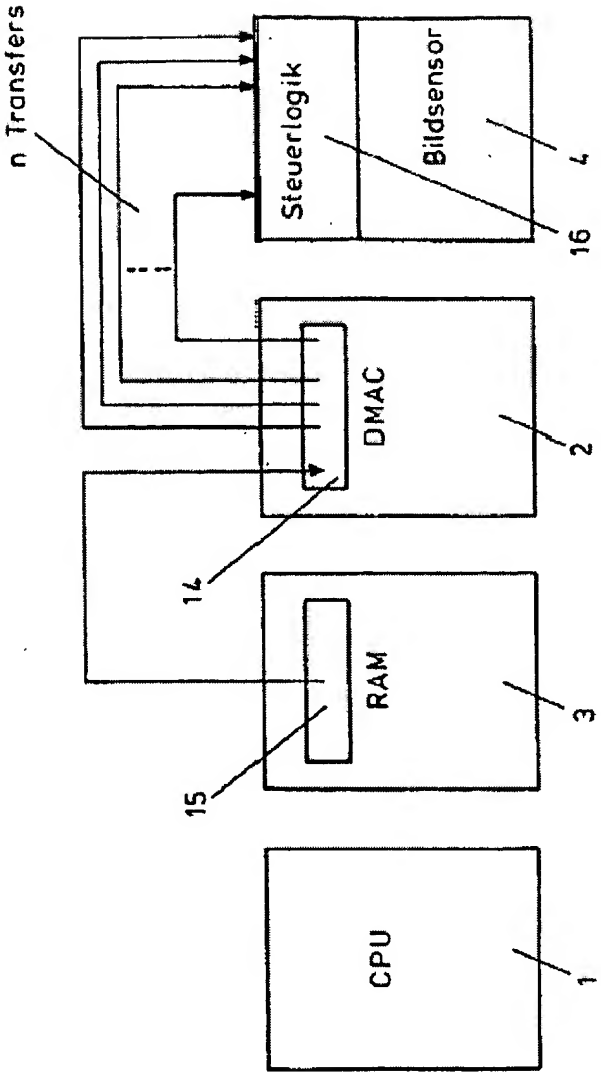
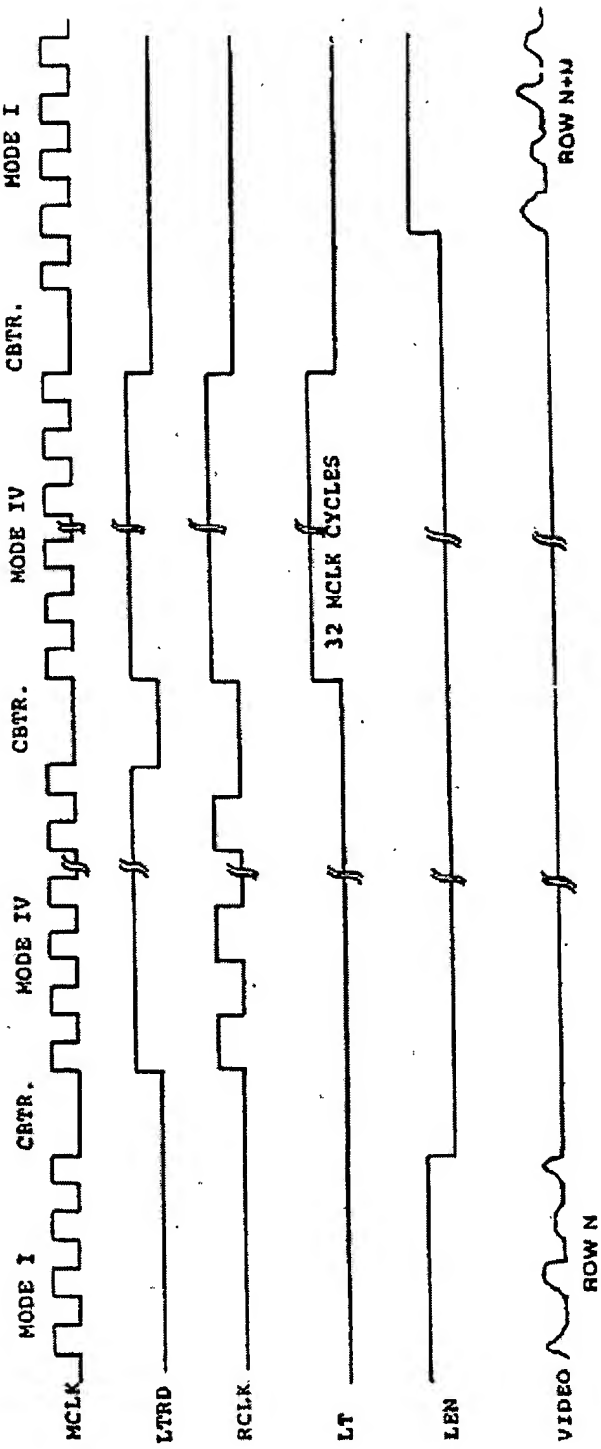


Fig. 3

n Transfers	=	n transfers
Steuerlogik	=	control logic
Bildsensor	=	image sensor



CBTR: Kommandoblock Transfer

Fig. 4

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Kommandoblock Transfer = Command block transfer